CLAIMS

What is claimed is:

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1. A method comprising:

trapping initializing data of a first interrupt type to a first interrupt controller;

re-routing the initializing data of the first interrupt type to a second interrupt controller; and

configuring the second interrupt controller to manage interrupts of the first interrupt type.

2. The method of claim 1, wherein trapping initializing data of a first interrupt type comprises:

configuring a system management interrupt to recognize initializing data of a first interrupt type.

3. The method of claim 1, wherein initializing data of the first interrupt type comprises a plurality of command words and a first command word begins the initializing of the first interrupt controller, configuring a system management interrupt to recognize initializing data of a first interrupt type and re-route initializing data to the second interrupt controller from the first command word.

4. The method of claim 1, wherein the first interrupt controller comprises an 82C59 controller and the second interrupt controller comprises a advanced programmable interrupt controller.

5. A machine readable storage media containing executable program instructions which when executed cause a digital processing system to perform a method comprising:

trapping initializing data of a first interrupt type to a first interrupt controller;

re-routing initializing data of a first interrupt type to a second interrupt controller; and

configuring the second interrupt controller to manage interrupts of the first interrupt type.

6. The media of claim 5, wherein trapping initializing data of a first interrupt type comprises:

configuring a system management interrupt to recognize initializing data of a first interrupt type.

7. The media of claim 5, wherein initializing data of the first interrupt type comprises a plurality of command words and a first command word begins the initializing of the first

interrupt controller, configuring a system management interrupt to recognize initializing data of a first interrupt type and re-route initializing data to the second interrupt controller from the first command word.

8. The media of claim 5, wherein the first interrupt controller comprises an 82C59 controller and the second interrupt controller comprises a advanced programmable interrupt controller.

9. A system comprising:

a central processing unit (CPU);

a first bus coupled to the CPU;

a first interrupt controller, coupled to the first bus, operable to manage communication with the CPU of interrupts of a first interrupt type;

a second bus coupled to the CPU;

a second interrupt controller, coupled to the second bus and to the first interrupt controller, operable to manage communication with the CPU of interrupts of a second interrupt type; and

a memory coupled to the second interrupt controller comprising a computer-readable medium having a computer-readable

program embodied therein for directing operation of the system, the computer-readable program comprising:

instructions for managing interrupts of the first interrupt type by the second interrupt controller.

10. The system of claim 9, wherein the computer-readable program further comprises:

instructions for trapping initializing data of a first interrupt type to the first interrupt controller;

instructions for re-routing initializing data of a first interrupt type to the second interrupt controller; and

instructions for configuring the second interrupt controller to manage interrupts of the first interrupt type.

11. The system of claim 10, wherein the instructions for trapping initializing data comprise:

instructions for configuring a system management interrupt to recognize initializing data of a first interrupt type.

12. The system of claim 10, wherein initializing data of the first interrupt type comprise a plurality of command words and a first command word begins the initializing of the first interrupt controller, and the computer-readable program comprises instructions for configuring a system management

interrupt to recognize initializing data of a first interrupt type and re-route initializing data to the second interrupt controller from the first command word.

13. The system of claim 9, wherein the first interrupt controller comprises an 82C59 controller and the second interrupt controller comprises a advanced programmable interrupt controller.

14. The system of claim 13, wherein the second interrupt controller manages interrupts of the first interrupt type exclusive of the first interrupt controller.

15. A system comprising:

a central processing unit (CPU);

first means of interrupt processing for managing communication with the CPU of interrupts of a first interrupt type;

second means of interrupt processing for managing communication with the CPU of interrupts of a second interrupt type;

means for routing interrupts of the first interrupt type to the second interrupt processing means

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means for managing interrupts of the first interrupt type by the second interrupt processing means exclusive of the first interrupt processing means.